STIC Search Report
EIC 2100

STIC Database Tracking Number: 141562

TO: Cam-Linh T Nguyen **Location: RND 3C21** **Art Unit : 2161** **Tuesday, January 04, 2005** **Case Serial Number: 09/284113**	**From: David Holloway** **Location: EIC 2100** **RND 4B19** **Phone: 2-3528** **david.holloway@uspto.gov**

Search Notes

Dear Examiner Nguyen,

Attached please find your search results for above-referenced case.
Please contact me if you have any questions or would like a re-focused search.

David

Access DB# _____

SEARCH REQUEST FORM

Scientific and Technical Information Center

Requester's Full Name: Nguyen, Cam Linh Examiner #: 78921 Date: 12/30/04
Art Unit: 2161 Phone Number 30 2-4024 Serial Number: 09/784,113
Mail Box and Bldg/Room Location: RND 3C21 Results Format Preferred (circle): PAPER DISK E-MAIL

If more than one search is submitted, please prioritize searches in order of need.

****

Please provide a detailed statement of the search topic, and describe as specifically as possible the subject matter to be searched. Include the elected species or structures, keywords, synonyms, acronyms, and registry numbers, and combine with the concept or utility of the invention. Define any terms that may have a special meaning. Give examples or relevant citations, authors, etc, if known. Please attach a copy of the cover sheet, pertinent claims, and abstract.

Title of Invention: System & method for Creating and Manipulating Information containers with Dynamic Registers

Inventors (please provide full names): DeAngelo, Michael

Earliest Priority Filing Date: 1/30/98

**For Sequence Searches Only* Please include all pertinent information (parent, child, divisional, or issued patent numbers) along with the appropriate serial number.*

See claims

****

STAFF USE ONLY	Type of Search		Vendors and cost where applicable	
Searcher: Linda Holloway	NA Sequence (#)		STN	
Searcher Phone #: 2-3528	AA Sequence (#)		Dialog	# 721
Searcher Location: RND 4B19	Structure (#)		Questel/Orbit	
Date Searcher Picked Up: 1-3-05	Bibliographic	✓	Dr.Link	
Date Completed: 1-4-05	Litigation		Lexis/Nexis	
Searcher Prep & Review Time: 50	Fulltext	✓	Sequence Systems	
Clerical Prep Time:	Patent Family		WWW/Internet	✓
Online Time: 150	Other		Other (specify)	

PTO-1590 (8-01)

```
Set     Items   Description
S1     272090   CONTAINER? OR ENVELOPE? OR BUCKET? OR (DATA OR INFORMATION-
            )()(ENCLOSURE? OR RECEPTACLE? OR FOLDER?)
S2     220678   REGISTER? OR REGISTR? OR (STORAGE OR MEMORY)(N)(LOCATION? -
            OR AREA OR AREAS OR ADDRESS? OR SECTOR? OR REGION?)
S3      19487   S2(2N)(MULTIPLE OR MULTIPLICITY OR PLURAL OR PLURALITY OR -
            MULTIPLICITY OR SEVERAL OR DIFFERENT OR MANY OR VARIOUS OR VA-
            RIETY)
S4        330   S3(5N)(ALTERABLE OR DYNAMIC? OR CHANGE? OR MODIFY? OR REVI-
            S? OR EDIT? OR LIVE OR HOT)
S5    1245365   TIME? OR SCHEDUL? OR HOUR? OR CALENDAR? OR TIMING OR TIMING
             OR DURATION? OR INTERVAL?
S6         87   S4(S)S5
S7         12   S1(10N)S3(10N)S5
S8          4   S1(S)S4(S)S5
S9         11   S6 AND IC=(G06F-017? OR G06F-007?)
S10        25   S7 OR S8 OR S9
S11        48   S6 AND IC=G06F?
S12        59   S10 OR S11
S13        42   S12 NOT AD=19980130:20010130
S14        36   S13 NOT AD=20010130:20030130
S15        35   S14 NOT AD=20030130:20050103
S16        11   S15 AND S1
S17        11   IDPAT (sorted in duplicate/non-duplicate order)
S18        11   IDPAT (primary/non-duplicate records only)
File 348:EUROPEAN PATENTS 1978-2004/Dec W03
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20041230,UT=20041223
         (c) 2004 WIPO/Univentio
```

18/3,K/2 (Item 2 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

00937647
System and method for parsing multiple sets of data
System und Verfahren zur Analyse mehrerer Datenmengen
Systeme et procede pour l'analyse de plusieurs ensembles de donnees
PATENT ASSIGNEE:
Hewlett-Packard Company, (206030), 3000 Hanover Street, Palo Alto, California 94304, (US), (Applicant designated States: all)
INVENTOR:
Pakenham, Gene, 5243 W 11th No. 1812, Greeley, Co 80634, (US)
DeVore, Darwin A., 1221 Eastlake Court, Loveland, CO 80537, (US)
LEGAL REPRESENTATIVE:
Carpmaels & Ransford (101821), 43 Bloomsbury Square, London WC1A 2RA, (GB)
PATENT (CC, No, Kind, Date): EP 853418 A2 980715 (Basic)
EP 853418 A3 000705
APPLICATION (CC, No, Date): EP 97309785 971204;
PRIORITY (CC, No, Date): US 782729 970113
DESIGNATED STATES: DE; FR; GB
EXTENDED DESIGNATED STATES: AL; LT; LV; MK; RO; SI
INTERNATIONAL PATENT CLASS: H04N-001/40; H04N-001/64
ABSTRACT WORD COUNT: 43
NOTE:
Figure number on first page: 1

LANGUAGE (Publication,Procedural,Application): English; English; English
FULLTEXT AVAILABILITY:

Available Text	Language	Update	Word Count
CLAIMS A	(English)	9829	351
SPEC A	(English)	9829	5723
Total word count - document A			6074
Total word count - document B			0
Total word count - documents A + B			6074

...SPECIFICATION from the CCD cells into a sequential or serial data stream.

A typical analog shift **register** comprises a **plurality** of "charge transfer **buckets** " each of which is connected to an individual cell. At the end of the exposure **time** , the charges collected by each of the CCD cells are simultaneously transferred to the charge transfer **buckets** , thus preparing the CCD cells for the next exposure sequence. The charge in each **bucket** is then transferred from **bucket** to **bucket** out of the shift register in a sequential or " **bucket** brigade" fashion during the time the CCD cells are being exposed to the next scan...

18/3,K/10 (Item 10 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00300850 **Image available**
UPDATE MECHANISM FOR COMPUTER STORAGE CONTAINER MANAGER
MOYEN DE MISE A JOUR POUR MODULE DE GESTION D'ELEMENTS DE STOCKAGE D'ORDINATEURS
Patent Applicant/Assignee:
APPLE COMPUTER INC,
Inventor(s):
HARRIS Jared M,
RUBEN Ira L,
Patent and Priority Information (Country, Number, Date):
Patent: WO 9519001 A1 19950713
Application: WO 95US196 19950104 (PCT/WO US9500196)
Priority Application: US 94177853 19940105
Designated States:
(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AM AT AU BB BG BR BY CA CH CN CZ DE DK EE ES FI GB GE HU JP KE KG KP KR KZ LK LR LT LU LV MD MG MN MW MX NL NO NZ PL PT RO RU SD SE SI SK TJ TT UA UZ VN KE MW SD SZ AT BE CH DE DK ES FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN ML MR NE SN TD TG
Publication Language: English
Fulltext Word Count: 119635

Fulltext Availability:
Claims

Claim
... the TOC and global name table of the target, Up to this point the updating **container** has basically been opened "normally" like any other. It has its own TOC and global...

...that will eventually be returned to the user will be the one for the updating **container** , so the targetFs TOC and global name table must be inherited by the updating CCB,
The way the updating **container** gets to use the ...simply to copy the target's TOC and global name table pointers into the updating **container** CCB, But the pointers to the tables already there can't simply be clobbered. They...

...global name table pointers used by everyone, and the "private" pair mainly used by close- **time** processing.
One other pointer is inherited. That is a pointer referred to as the "target **container** pointer" (targetContainer), It is a CCB pointer copied from the target. It is always initialized...

...both "All and "B"s targetContainer will point to "B", This pointer is used for **container** refNum validity checks in the various API routines, It is the opposite of the updatingContainer pointer mentioned in step (1). updatingContainer points to the top-most **container** , and targetContainer the bottom-most (final or ultimate target).
(5). Load in updater's non-private TOC
If this is a previously existing updating **container** opened for reading, then it is at this point all the updates from the updating **container** are applied to the target, The non-private portion of the updating **container** 's TOC was loaded first in step (3),

Since the normal TOC is now the...

...updating" list properties for the objects they update will be encountered. As discussed for close- **time** processing, these will be value operations (set-infos, data edits, moves, etc.). The value data...

...represent all objects needing updating. The touched chain can now be walked much like close- **time** processing to process the updating instructions associated with the "updating" property of each object on the chain. Also like close- **time** processing, objects on the touched chain are removed from the chain after each updating list...

...size and offsets are generated for the value headers and segments. Applying updates at this **time** changes the logical sizes and offsets. Thus, after each value's updates are completed, if...

...the value must be "re-logicalized". It should also be pointed out that during this **time** , recording of updates is suppressed. It stays suppressed until the end of all open processing...

...and property updating instructions can be processed using the special TOC #1 property of the **container** 's private TOC. At this point the target And the updating **container** have been opened, The updater's CCB pointer is returned to the user as the **container** refNum, The diagram of Fig. 22 illustrates the pertinent data structures discussed above. In the...

...target point to the same tables. Since "All is opened first, then "B". the close- **time** processing reverses this by closing "B" then "A", In order to prevent the closing of...

...the TOC and global name tables. This prevents premature release of the data.

H. Open- **time** Processing for Multi-layered Updaters

The previous discussion was mainly limited to one **container** updating another, It is fairly simple extension to the algorithm to allow for multiple updaters. Multiple updaters arise if a new **container** is opened for updating a target in multiple sessions. For example, the above situation was other hand, there is nothing preventing another new updating **container** from being opened,, say "XI', and using "All as its target; IIX updating "All updating...

...The process is the same, except for one variation in step (3) of the open- **time** processing; opening of the target **container** . Basically, as part of standard open- **time** processing, a check is always made to see if TOC #1 has a "Pointing value". This only exists in updating **container** TOCs and allows access to the proper target, be it separate or appended. If the...

...TOC is present in memory that is indistinguishable from that of an ordinary, non-update **container** , except that some of the values refer to data actually present in other **containers** . Each of the **containers** in the update chain remain open

so that value operations can reach the data,
I...

...Appendix D is a C-language header file for routines which read and write the **container** TOC. Appendix E sets forth the routines themselves, Appendix F is a C-language header file for a set of basic **container** handlers, and their metahandler, used by the **Container** Manager when doing update operations on a target **container** . Appendix G sets forth the handlers themselves.
The foregoing description of preferred embodiments of the...

...to
practitioners skilled in this art. As one example, an embodiment may permit an update **container** to be an update of two or more target **containers** concurrently, As another example, an implementation of the routines may construct only those aspects of the TOC in-memory which are needed for a particular operation after an update **container** is opened. The embodiments described herein were chosen and described in order to best explain...

```
Set     Items   Description
S1     905852   CONTAINER? OR ENVELOPE? OR BUCKET? OR (DATA OR INFORMATION-
            )()(ENCLOSURE? OR RECEPTACLE? OR FOLDER?)
S2    3635562   REGISTER? OR REGISTR? OR (STORAGE OR MEMORY)(N)(LOCATION? -
            OR AREA OR AREAS OR ADDRESS? OR SECTOR? OR REGION?)
S3      38232   S2(3N)(MULTIPLE OR MULTIPLICITY OR PLURAL OR PLURALITY OR -
            MULTIPLICITY OR SEVERAL OR DIFFERENT OR MANY OR VARIOUS OR VA-
            RIETY)
S4     142842   S2(5N)(ALTERABLE OR DYNAMIC? OR CHANGE? OR MODIFY? OR REVI-
            S? OR EDIT? OR LIVE OR HOT)
S5      50584   S1(12N)(TIME? OR SCHEDUL? OR HOUR? OR CALENDAR? OR TIMING -
            OR TIMING OR DURATION? OR INTERVAL?)
S6          0   S3(S)S4(S)S5
S7          6   S4(S)S5
S8          4   S3(S)S5
S9        570   S2(S)S5
S10       210   S2(10N)S5
S11         5   S10(10N)(ALTERABLE OR DYNAMIC? OR CHANGE? OR MODIFY? OR RE-
            VIS? OR EDIT? OR LIVE OR HOT)
S12        15   S11 OR S8 OR S7
S13         9   RD (unique items)
S14       146   S2(5N)S5
S15        57   S14(S)(DATA OR BIT OR BYTE? OR DATABLOCK? OR INFORMATION? -
            OR MEMOR? OR STORAGE? OR BUFFER? OR CACHE?)
S16        37   RD (unique items)
S17        45   S16 OR S13
S18        45   RD (unique items)
S19        23   S18 NOT PY>1998
S20        21   S19 NOT PD=19980130:20010130
S21        21   S20 NOT PD=20010130:20050110
File 275:Gale Group Computer DB(TM) 1983-2005/Jan 04
         (c) 2005 The Gale Group
File  47:Gale Group Magazine DB(TM) 1959-2005/Jan 04
         (c) 2005 The Gale group
File  75:TGG Management Contents(R) 86-2004/Dec W1
         (c) 2004 The Gale Group
File 636:Gale Group Newsletter DB(TM) 1987-2005/Jan 04
         (c) 2005 The Gale Group
File  16:Gale Group PROMT(R) 1990-2005/Jan 04
         (c) 2005 The Gale Group
File 624:McGraw-Hill Publications 1985-2004/Dec 28
         (c) 2004 McGraw-Hill Co. Inc
File 484:Periodical Abs Plustext 1986-2004/Dec W4
         (c) 2004 ProQuest
File 613:PR Newswire 1999-2005/Jan 03
         (c) 2005 PR Newswire Association Inc
File 813:PR Newswire 1987-1999/Apr 30
         (c) 1999 PR Newswire Association Inc
File 141:Readers Guide 1983-2004/Sep
         (c) 2004 The HW Wilson Co
File 370:Science 1996-1999/Jul W3
         (c) 1999 AAAS
File 696:DIALOG Telecom. Newsletters 1995-2005/Jan 03
         (c) 2005 The Dialog Corp.
File 553:Wilson Bus. Abs. FullText 1982-2004/Sep
         (c) 2004 The HW Wilson Co
File 621:Gale Group New Prod.Annou.(R) 1985-2005/Jan 04
         (c) 2005 The Gale Group
File 674:Computer News Fulltext 1989-2004/Dec W2
         (c) 2004 IDG Communications
File  88:Gale Group Business A.R.T.S. 1976-2005/Dec 30
         (c) 2005 The Gale Group
File 369:New Scientist 1994-2004/Dec W3
         (c) 2004 Reed Business Information Ltd.
File 160:Gale Group PROMT(R) 1972-1989
         (c) 1999 The Gale Group
File 635:Business Dateline(R) 1985-2005/Jan 01
         (c) 2005 ProQuest Info&Learning
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File 15:ABI/Inform(R) 1971-2005/Jan 01
(c) 2005 ProQuest Info&Learning
File 9:Business & Industry(R) Jul/1994-2005/Jan 03
(c) 2005 The Gale Group
File 13:BAMP 2005/Dec W4
(c) 2005 The Gale Group
File 810:Business Wire 1986-1999/Feb 28
(c) 1999 Business Wire
File 610:Business Wire 1999-2005/Jan 03
(c) 2005 Business Wire.
File 647:CMP Computer Fulltext 1988-2005/Dec W3
(c) 2005 CMP Media, LLC
File 98:General Sci Abs/Full-Text 1984-2004/Sep
(c) 2004 The HW Wilson Co.
File 148:Gale Group Trade & Industry DB 1976-2004/Jan 03
(c)2004 The Gale Group
File 634:San Jose Mercury Jun 1985-2004/Dec 31
(c) 2005 San Jose Mercury News

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Set     Items   Description
S1     325405   CONTAINER? OR ENVELOPE? OR BUCKET? OR (DATA OR INFORMATION-
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S2     304185   REGISTER? OR REGISTR? OR (STORAGE OR MEMORY)(N)(LOCATION? -
            OR AREA OR AREAS OR ADDRESS? OR SECTOR? OR REGION?)
S3       5930   S2(2N)(MULTIPLE OR MULTIPLICITY OR PLURAL OR PLURALITY OR -
            MULTIPLICITY OR SEVERAL OR DIFFERENT OR MANY OR VARIOUS OR VA-
            RIETY)
S4         91   S3(5N)(ALTERABLE OR DYNAMIC? OR CHANGE? OR MODIFY? OR REVI-
            S? OR EDIT? OR LIVE OR HOT)
S5    8070002   TIME? OR SCHEDUL? OR HOUR? OR CALENDAR? OR TIMING OR TIMING
             OR DURATION? OR INTERVAL?
S6          1   S1 AND S4
S7      56519   S1 AND S5
S8         11   S3 AND S7
S9         36   S1 AND S3
S10        36   S6 OR S8 OR S9
S11        27   RD (unique items)
S12       445   S1 AND S2 AND S5
S13      8654   S1(3N)(DATA OR INFORMATION OR BYTE? OR BITS OR MEGABYTE? OR
             KILOBYTE? OR STORAGE? OR MEMORY?)
S14        49   S12 AND S13
S15        74   S14 OR S11
S16        65   RD (unique items)
S17        49   S16 NOT PY>1998
File   8:Ei Compendex(R) 1970-2005/Dec W4
         (c) 2005 Elsevier Eng.  Info. Inc.
File  35:Dissertation Abs Online 1861-2004/Dec
         (c) 2004 ProQuest Info&Learning
File  65:Inside Conferences 1993-2004/Dec W4
         (c) 2004 BLDSC all rts. reserv.
File   2:INSPEC 1969-2004/Dec W2
         (c) 2004 Institution of Electrical Engineers
File  94:JICST-EPlus 1985-2004/Nov W4
         (c)2004 Japan Science and Tech Corp(JST)
File 111:TGG Natl.Newspaper Index(SM) 1979-2004/Dec 29
         (c) 2004 The Gale Group
File   6:NTIS 1964-2004/Dec W4
         (c) 2004 NTIS, Intl Cpyrght All Rights Res
File 144:Pascal 1973-2004/Dec W1
         (c) 2004 INIST/CNRS
File 434:SciSearch(R) Cited Ref Sci 1974-1989/Dec
         (c) 1998 Inst for Sci Info
File  34:SciSearch(R) Cited Ref Sci 1990-2004/Dec W4
         (c) 2004 Inst for Sci Info
File  99:Wilson Appl. Sci & Tech Abs 1983-2004/Nov
         (c) 2004 The HW Wilson Co.
File  95:TEME-Technology & Management 1989-2004/Jun W1
         (c) 2004 FIZ TECHNIK
```

17/5/13 (Item 13 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

00267759 E.I. Monthly No: EI7212010596
Title: SIMPLE CHARGE REGENERATOR FOR USE WITH CHARGE-TRANSFER DEVICES AND THE DESIGN OF FUNCTIONAL LOGIC ARRAYS.
Author: Tompsett, Michael F.
Corporate Source: Bell Telephone Lab, Inc, Murray Hill, NJ
Source: IEEE Journal of Solid-State Circuits v SC-7 n 3 Jun 1972 p 237-242
Publication Year: 1972
CODEN: IJSCBC ISSN: 0018-9200
Language: ENGLISH
Journal Announcement: 7212
Abstract: An inverting binary-charge regenerator for use with new charge-transfer devices (charge-coupled and integrated MOS **bucket** brigade) is described. This simple element requires an area approximately that of one bit in the register and is driven by the transfer pulses. Its uses with these shift **registers** in **various** configurations, which are described, make possible even larger functional devices. These uses include regeneration in serial memories, performing logic operations such as NAND and NOR involving the bit trains in **several** **registers** , and performing fixed counts and sequential addressing of other circuit elements.
Descriptors: *LOGIC CIRCUITS
Classification Codes:
721 (Computer Circuits & Logic Elements)
72 (COMPUTERS & DATA PROCESSING)

17/5/17 (Item 4 from file: 35)
DIALOG(R)File 35:Dissertation Abs Online

01219256 ORDER NO: AAD92-14527

ANALYTICAL MODELS AND OPTIMAL STRATEGIES FOR AUTOMATED STORAGE/RETRIEVAL SYSTEM OPERATIONS (STORAGE-RETRIEVAL)

Author: PARK, BYUNG CHUN
Degree: PH.D.
Year: 1991
Corporate Source/Institution: GEORGIA INSTITUTE OF TECHNOLOGY (0078)
Director: EDWARD H. FRAZELLE
Source: VOLUME 52/12-B OF DISSERTATION ABSTRACTS INTERNATIONAL.
PAGE 6592. 184 PAGES
Descriptors: ENGINEERING, INDUSTRIAL
Descriptor Codes: 0546

The objective of this research is to provide exact reliable expressions for use in designing and operating automated storage/retrieval systems. We focus on the efficient operation of dual command cycles. The main performance criteria are travel **time** and system throughput.

We begin by developing a general analytical baseline for automated storage/retrieval system performance analysis. The baseline is a closed-form expression for the mean and variance of single and dual command cycle **time** . The model can be effectively used for evaluating any storage policy, i.e., random, dedicated or class-based storage. We give examples to illustrate how the formulas can be used for evaluating each storage policy.

With an evaluation baseline, our attention turns to specific improvement strategies. Contour line configurations for **storage location** assignment are developed first. We develop a general scheme to generate contour line configurations for dual command operations. To investigate the effects of alternative contour line configurations on system performance, a series of experiments are performed. The storage policies considered are random storage, priority-based open location (POL) storage, turnover-based storage, and 2-class storage. The performance of each contour line configuration is measured in terms of the expected dual command travel **time** .

Next, we develop optimal dwell point policies for automated storage/retrieval systems. Based on the fact that dwell point policies minimize the completion **time** of the first transaction after the storage/retrieval machine becomes idle, we show that there is a unique optimal dwell point policy, regardless of other system parameters. Then a variety of return paths to the dwell point are introduced and studied.

Finally, an end-of-aisle order picking system with inbound and outbound buffer positions is studied. This is usually referred to as a miniload system with a horse-shoe "front-end". The system is modeled as a two-stage cyclic queueing system consisting of one general and one exponential server with limited capacity. The cyclic queueing system is then analyzed by using the customer-hole duality concept. Closed-form expressions for the stationary probability and system throughput are developed. We also obtain the proportion of picker-idle and storage/retrieval machine-idle **time** by noting that the throughput of the picker is equal to that of the storage/retrieval machine. Then, a design problem to determine the optimal number of inbound and outbound buffer positions and a control problem to determine the optimal number of **storage containers** in the system are studied. The effect of buffer size on system throughput is also investigated.

```
Set     Items   Description
S1     675611   CONTAINER? OR ENVELOPE? OR BUCKET? OR (DATA OR INFORMATION-
            )()(ENCLOSURE? OR RECEPTACLE? OR FOLDER?)
S2     397825   REGISTER? OR REGISTR? OR (STORAGE OR MEMORY)(N)(LOCATION? -
            OR AREA OR AREAS OR ADDRESS? OR SECTOR? OR REGION?)
S3      12040   S2(2N)(MULTIPLE OR MULTIPLICITY OR PLURAL OR PLURALITY OR -
            MULTIPLICITY OR SEVERAL OR DIFFERENT OR MANY OR VARIOUS OR VA-
            RIETY)
S4        140   S3(5N)(ALTERABLE OR DYNAMIC? OR CHANGE? OR MODIFY? OR REVI-
            S? OR EDIT? OR LIVE OR HOT)
S5    3326894   TIME? OR SCHEDUL? OR HOUR? OR CALENDAR? OR TIMING OR TIME(-
            )STAMP?
S6         34   S4 AND S5
S7          0   S1 AND S4
S8         70   S1 AND S3
S9          5   S8 AND IC=(G06F-017? OR G06F-007?)
S10        11   S8 AND IC=G06F?
S11        20   S4 AND IC=(G06F-017? OR G06F-007?)
S12        22   S6 AND IC=G06F?
S13     88865   MC=(T01-C04? OR T01-J05B?)
S14         5   S13 AND (S6 OR S8)
S15        40   S12 OR S11 OR S14
S16        40   IDPAT (sorted in duplicate/non-duplicate order)
S17        39   IDPAT (primary/non-duplicate records only)
File 347:JAPIO Nov 1976-2004/Aug(Updated 041203)
         (c) 2004 JPO & JAPIO
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200482
         (c) 2004  Thomson Derwent
```

17/5/3 **(Item 3 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

015947975 **Image available**
WPI Acc No: 2004-105816/200411
Method and system for vector scheduling **on object code level**
Patent Assignee: UNIV INHA (UYIN-N)
Inventor: KIM G C; KIM J S; KIM S D; LEE D H; LEE Y S
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
KR 2003078467	A	20031008	KR 200217526	A	20020329	200411	B

Priority Applications (No Type Date): KR 200217526 A 20020329
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
KR 2003078467	A		1	G06F-009/38	

Abstract (Basic): KR 2003078467 A
NOVELTY - A method and a system for vector **scheduling** on an object code level are provided to produce an excellent **scheduling** result in a **scheduling time** faster than a present software pipelining method.
DETAILED DESCRIPTION - An LCV(Loop Control Variable), and an initialization instruction, an initial value, a change instruction, a variance width, and an end instruction of the LCV are found out by using a CFG(Control Flow Graph) of a vector loop as input. The number of the concurrent executing instructions is calculated and the copies are generated by developing the vector loop with x. Registers are renamed in order to remove the data dependency of the registers used for each copy. The LCV of the copies is **changed** to the **register different** with each other. The LCV initialization instruction in the copies is changed based on the variance width. The LCV changing instruction in the copies is changed based on the x value. The instruction for copying the value of the LCV to the variable is inserted into a loop termination path of the copies. The vector **scheduled** CFG is generated by collecting the duplicated instruction for each instruction of the first copy.
pp; 1 DwgNo 1/10
Title Terms: METHOD; SYSTEM; VECTOR; **SCHEDULE** ; OBJECT; CODE; LEVEL
Derwent Class: T01
International Patent Class (Main): **G06F-009/38**
File Segment: EPI

17/5/5 **(Item 5 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

015768651 **Image available**
WPI Acc No: 2003-830853/200377
XRPX Acc No: N03-663897

Dynamic random access memory controller in computer system, has configuration registers to store control information of memory banks, and column address strobe state machine to generate strobe signals for memory banks

Patent Assignee: INTEL CORP (ITLC)
Inventor: LANGENDORF B K; DODD J M; WADE N D

Number of Countries: 001 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
US 20030177303	A1	20030918	US 97814697	A	19970311	200377 B
			US 2003389092	A	20030313	
US 6725349	B2	20040420	US 94381091	A	19941223	200427
			US 97814697	A	19970311	
			US 2003389092	A	20030313	

Priority Applications (No Type Date): US 97814697 A 19970311; US 2003389092 A 20030313; US 94381091 A 19941223
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 20030177303	A1		10	G06F-012/00	Cont of application US 97814697
US 6725349	B2			G06F-012/00	Cont of application US 94381091
					Cont of application US 97814697

Abstract (Basic): US 20030177303 A1

NOVELTY - **Several** configuration **registers** (300) store control information for **dynamic** RAM (DRAM) memory banks of a main memory (103). A column address strobe (CAS) state machine (330) coupled to the registers, generates CAS signals (220) for the memory banks. A detection logic circuit coupled to the CAS state machine, determines type of DRAM device installed in each memory bank to store control information of the device in the registers.

DETAILED DESCRIPTION - An INDEPENDENT CLAIM is also included for method for optimizing control of each memory bank.

USE - For automatically configuring and controlling memory banks installed with dynamic random access memory (DRAM) devices including standard page mode DRAM and extended data-out DRAM (EDO-DRAM) in computer system.

ADVANTAGE - The CAS state machine automatically controls **timing** requirements of the DRAM devices installed in the main memory to quickly and efficiently handle access requests. Thus, the performance of EDO-DRAM and standard page mode DRAM is preserved and controlled without increasing the hardware cost, while ensuring correct operation of the DRAMs.

DESCRIPTION OF DRAWING(S) - The figure shows the block diagram of the DRAM controller.

main memory (103)
CAS signals (220)
configuration register (300)
address bank decoder (310)
CAS state machine (320)
pp; 10 DwgNo 3/7

Title Terms: DYNAMIC; RANDOM; ACCESS; MEMORY; CONTROL; COMPUTER; SYSTEM; CONFIGURATION; REGISTER; STORAGE; CONTROL; INFORMATION; MEMORY; BANK; COLUMN; ADDRESS; STROBE; STATE; MACHINE; GENERATE; STROBE; SIGNAL; MEMORY ; BANK

Derwent Class: T01; U14
International Patent Class (Main): **G06F-012/00**
File Segment: EPI

17/5/11 **(Item 11 from file: 350)**
DIALOG(R)File 350:Derwent WPIX

013483279 **Image available**
WPI Acc No: 2000-655222/200063
Related WPI Acc No: 1999-457716
XRPX Acc No: N00-485639

Data processing system used in graphical user interface, displays one of subset of stored object automatically only if at least one of stored object of subset has not been manually associated with its container

Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: LISLE L A; MARTIN S L; MULLALY J M
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
US 6104394	A	20000815	US 97813717	A	19970307	200063	B
			US 99239405	A	19990128		

Priority Applications (No Type Date): US 97813717 A 19970307; US 99239405 A 19990128
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
US 6104394	A		19	G06F-017/30	Cont of application US 97813717 Cont of patent US 5936624

Abstract (Basic): US 6104394 A

NOVELTY - Two subsets constituting stored object of respective object types within respective **containers** , are displayed automatically in a display unit, only if at least one of stored objects of the two subsets has not been manually associated with their respective **containers** .

DETAILED DESCRIPTION - The display unit automatically updates the displayed subsets when the stored objects is charged, when either storing, editing, deleting, moving, archiving, copying, linking on undoing of stored object occurs. The object type is chosen from text type, audio type, graphic type, type corresponding to date and time. INDEPENDENT CLAIMS are also included for the following:

(a) operating data processing system;

(b) program product

USE - Used in graphical user interface, real world style interface with logical containment system.

ADVANTAGE - Enables user to organize representation of desired objects in **various storage locations** without requiring extra steps by a user access memory. Allows greater flexibility in obtaining desired graphical user interface, by the ability of user to modify the containment settings and to have modifications immediately rejected in logical **container** rendered on display device.

DESCRIPTION OF DRAWING(S) - The figure shows model diagram of data processing system explained with Booch notation.

pp; 19 DwgNo 8/8

Title Terms: DATA; PROCESS; SYSTEM; GRAPHICAL; USER; INTERFACE; DISPLAY; ONE; SUBSET; STORAGE; OBJECT; AUTOMATIC; ONE; STORAGE; OBJECT; SUBSET; MANUAL; ASSOCIATE; **CONTAINER**
Derwent Class: T01
International Patent Class (Main): G06F-017/30
File Segment: EPI

17/5/22 (Item 22 from file: 350)
DIALOG(R)File 350:Derwent WPIX

007659045 **Image available**
WPI Acc No: 1988-292977/198841
XRPX Acc No: N88-222362

Multiprocessor system with shared memory - has machine instruction sequence in shared memory for assigning register sets based on status information

Patent Assignee: STELLAR COMPUTER IN (STEL-N)
Inventor: DARNELL P A; MORTON M A

Number of Countries: 029 Number of Patents: 002
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week
WO 8807720	A	19881006	WO.88US1032	A	19880325	198841 B
AU 8816821	A	19881102				198904

Priority Applications (No Type Date): US 8734166 A 19870402
Cited Patents: 1.Jnl.Ref; EP 174446; US 3916383; US 3972029; US 3980922; US 4121286; US 4197579; US 4280176; US 4354227; US 4713757
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 8807720	A	E	27		

Designated States (National): AU BB BG BR DK FI HU JP KP KR LK MC MG MW NO RO SD SU
Designated States (Regional): AT BE CH DE FR GB IT LU NL OA SE

Abstract (Basic): WO 8807720 A

The multiprocessor system has four processors which share machine instruction sequence (14) stored in parallel regions in the memory (16), which includes parallel regions of instructions. Each region has two blocks of instructions which are independent in that the same result is obtained if the blocks are executed by the same processor or by different processors.

The system provides a pool (22) of high speed register sets to regulate the work of the four processors. Each processor has a respective unshared register (40) which stores a program status word. The word provides information about the part of the process executing on a given processor at a given **time** .

ADVANTAGE - The assignment of shared **register** sets to **multiple** processors is effected **dynamically** without interrupting the execution of instructions in the sequence.

1/8

Title Terms: MULTIPROCESSOR; SYSTEM; SHARE; MEMORY; MACHINE; INSTRUCTION; SEQUENCE; SHARE; MEMORY; ASSIGN; REGISTER; SET; BASED; STATUS; INFORMATION
Derwent Class: T01
International Patent Class (Additional): **G06F-012/00**
File Segment: EPI

07054897 **Image available**

COMMUNICATION INSTRUCTION RESULT OF PROCESSOR AND COMPILING METHOD FOR PROCESSOR

PUB. NO.: 2001-282532 [JP 2001282532 A]
PUBLISHED: October 12, 2001 (20011012)
INVENTOR(s): TOPHAM NIGEL PETER
APPLICANT(s): SIROYAN LTD
APPL. NO.: 2001-032090 [JP 200132090]
FILED: February 08, 2001 (20010208)
PRIORITY: 00 200002848 [GB 20002848], GB (United Kingdom), February 08, 2000 (20000208)
INTL CLASS: **G06F-009/38** ; **G06F-009/30** ; **G06F-009/34** ; **G06F-009/45**

ABSTRACT

PROBLEM TO BE SOLVED: To simplify a task of a compiler for the allocation of a register and to set up an instruction in a more compact state.

SOLUTION: A processor 1 for executing a pipeline by software includes an instruction issuing device 10 for issuing plural instructions to be executed by a previously determined sequence. The sequence of instructions includes plural value generation instructions for generating respective values at the **time** of execution of the sequence. Each of instruction execution devices 14, 16, 18 executes an issued instruction. A register file 20 has plural registers and stores plural values generated by respective executed instructions. During the period of operation, the processor 1 allocates plural values generated by respective value generation instructions to respective sequence numbers in accordance with the issued order of respective value generation instructions. Each generated value is allocated to one of plural registers in order to store the generated value on the basis of the sequence number allocated to the value. The names of these **plural registers** can be **changed** in each issue of a value generation instruction.

17/5/31 (Item 31 from file: 347)
DIALOG(R)File 347:JAPIO

03475828 **Image available**
DIGITAL PROCESSOR

PUB. NO.: 03-138728 [JP 3138728 A]
PUBLISHED: June 13, 1991 (19910613)
INVENTOR(s): SATOMURA RYUICHI
TOMOBE KATSUICHI
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 01-275821 [JP 89275821]
FILED: October 25, 1989 (19891025)
INTL CLASS: [5] **G06F-009/38**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JAPIO KEYWORD: R131 (INFORMATION PROCESSING -- Microcomputers & Microprocessers)
JOURNAL: Section: P, Section No. 1250, Vol. 15, No. 360, Pg. 105, September 11, 1991 (19910911)

ABSTRACT

PURPOSE: To shorten the instruction execution **time** of a microprocessor, etc., and to raise processing capacity by **dynamically** assigning **plural** work **registers** in accordance with its usage condition.

CONSTITUTION: n numbers of work registers WR1-WRn used when execution a micro-instruction, and a work register control part WRC which dynamically assigns these work registers WR1-WRn in accordance with their usage condition, are provided. Then, the work registers WR1-WRn can be dynamically assigned in accordance with their usage condition without specifying them with a micro-instruction, the score boarding of the work registers WR1-WRn can be executed simultaneously with the score boarding of a general purpose register GR by a machine language instruction, and the parallel processing of he following machine language instructions can be started early. Thus, the instruction execution **time** of the microprocessor, etc., can be shortened equally, and its processing capacity can be raised.

01917037 **Image available**

CONTINUOUS GENERATING SYSTEM OF PLURAL ADDRESSES

PUB. NO.: 61-131137 [JP 61131137 A]
PUBLISHED: June 18, 1986 (19860618)
INVENTOR(s): AKIBA HIROSHI
AOYANAGI KEIZO
APPLICANT(s): TOSHIBA CORP [000307] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 59-253342 [JP 84253342]
FILED: November 30, 1984 (19841130)
INTL CLASS: [4] **G06F-012/02**
JAPIO CLASS: 45.2 (INFORMATION PROCESSING -- Memory Units)
JOURNAL: Section: P, Section No. 512, Vol. 10, No. 324, Pg. 91, November 05, 1986 (19861105)

ABSTRACT

PURPOSE: To attain count-up or count-down sequentially for **plural** address **registers** by using an adder to **modify** logically an address of an address register before one address and applying it sequentially to each register.

CONSTITUTION: An address modification data and a logical address from an adder 2 inputting an addend for modification and generating a logical address are inputted sequentially to plural address registers 3,4,5. Then address information of the address registers 3,4,5 is selected in the predetermined order by a selector 10 and outputs it as a memory access (f). Further, the address register selected precedingly by the selector 10 is selected by the other selector 9 at the same **time** and the address information (e) is fed back to a selector 6 as the address modification data. Then a required addition is executed by the adder 2 to modify the address of the register subject to feed back. The operation is executed sequentially to the registers 3,4,5 to generate continuously plural addresses thereby clearing them.

17/5/37 **(Item 37 from file: 347)**
DIALOG(R)File 347:JAPIO

01655844 **Image available**
GUIDANCE INFORMATION CONTROLLING SYSTEM

PUB. NO.: 60-134344 [JP 60134344 A]
PUBLISHED: July 17, 1985 (19850717)
INVENTOR(s): YOSHINO ISAO
SOMA MASATO
APPLICANT(s): HITACHI LTD [000510] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 58-241921 [JP 83241921]
FILED: December 23, 1983 (19831223)
INTL CLASS: [4] **G06F-009/00** ; **G06F-015/00**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units); 45.4 (INFORMATION PROCESSING -- Computer Applications)
JOURNAL: Section: P, Section No. 408, Vol. 09, No. 299, Pg. 50, November 27, 1985 (19851127)

ABSTRACT

PURPOSE: To execute a change which requires no person's help by executing the change by sending guidance information to a terminal control device from a central processor by a guidance information change request from a change request mechanism of the central processor or a terminal equipment.

CONSTITUTION: A central processor 11, terminal control device 16 and a terminal equipment 20 are connected, a local guidance control mechanism 12 and a **timer** 13 are provided on the processor 11, and a storage mechanism 15 and a managing mechanism 14 are provided on the mechanism 12. Also, a local guidance change control mechanism 19 consisting of a store part 17 and a change identifying mechanism 18 is provided on the device 16, and the store part 17 is constituted of **plural storage area** 21 and on-demand **changeable** storage areas 22. In this state, the area 21 is changed by receiving a change request from the **timer** 13 by the mechanism 14 and sending retrieved information to the mechanism 19, a change request from the equipment 20 is registered in the mechanism 18 and also transferred to the processor 11, and the area 22 is changed by sending the retrieved information to the mechanism 19.

17/5/38 **(Item 38 from file: 347)**
DIALOG(R)File 347:JAPIO

01125342 **Image available**

OPERATION PROCESSING DEVICE

PUB. NO.: 58-062742 [JP 58062742 A]
PUBLISHED: April 14, 1983 (19830414)
INVENTOR(s): TAMURA NOBORU
APPLICANT(s): CANON INC [000100] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 56-162367 [JP 81162367]
FILED: October 12, 1981 (19811012)
INTL CLASS: [3] **G06F-007/00**
JAPIO CLASS: 45.1 (INFORMATION PROCESSING -- Arithmetic Sequence Units)
JOURNAL: Section: P, Section No. 208, Vol. 07, No. 152, Pg. 39, July 05, 1983 (19830705)

ABSTRACT

PURPOSE: To make the operation easy, by providing a means having a **plurality** of condition **registers** and storing the **change** in the condition codes in the past, and a means performing the operation instruction between condition registers.

CONSTITUTION: In executing an arithmetic logical operation instruction having the alteration of a CCR through the instruction of an instruction decoder 6, the conditions with the result of operation are set to the CCR. An arithmetic logical operation device 3 reads out the 1st CCR4-1 in one machine cycle and gives an output to the 2nd CCR4-2 in the next machine cycle. The conditions through the result of present operation are outputted to the 1st CCR4-1 in the next machine cycle. Through this operation, the previous condition is set to the 2nd CCTR4-2 and the present condition is set to the 1st CCR4-1. Further, with the operation instruction between the CCRs, the two CCRs 4-1, 4-2 are read and an output is given to the instructed CCR

```
Set     Items   Description
S1          9   AU=(DEANGELO, M? OR DEANGELO M? OR DE ANGELO M? OR DE ANGE-
             LO, M?)
S2          3   S1 AND IC=G06F?
File 347:JAPIO Nov 1976-2004/Aug(Updated 041203)
         (c) 2004 JPO & JAPIO
File 348:EUROPEAN PATENTS 1978-2004/Dec W03
         (c) 2004 European Patent Office
File 349:PCT FULLTEXT 1979-2002/UB=20041230,UT=20041223
         (c) 2004 WIPO/Univentio
File 350:Derwent WPIX 1963-2004/UD,UM &UP=200482
         (c) 2004  Thomson Derwent
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2/5/1 (Item 1 from file: 348)
DIALOG(R)File 348:EUROPEAN PATENTS

01077982
SYSTEM AND METHOD FOR CREATING AND MANIPULATING INFORMATION CONTAINERS WITH DYNAMIC REGISTERS
SYSTEM UND VERFAHREN ZUR ERZEUGUNG UND BEARBEITUNG VON INFORMATIONSBEHALTERN MITDYNAMISCHEN REGISTERN.
SYSTEME ET PROCEDE POUR LA CREATION ET LA MANIPULATION DE CONTENEURS D'INFORMATIONS A REGISTRES DYNAMIQUES
PATENT ASSIGNEE:
Ematrix Corporation, (2819080), 104 West Anapamu, Santa Barbara, CA 93101 , (US), (Applicant designated States: all)
INVENTOR:
De Angelo, Michael , Suite 290, 1324 J State Street, Santa Barbara, CA 93101, (US
LEGAL REPRESENTATIVE:
McLeish, Nicholas Alistair Maxwell et al (74621), Boult Wade Tennant Verulam Gardens 70 Gray's Inn Road, London WC1X 8BT, (GB)
PATENT (CC, No, Kind, Date): EP 1049996 A1 001108 (Basic)
WO 9939285 990805
APPLICATION (CC, No, Date): EP 99905548 990128; WO 99US1988 990128
PRIORITY (CC, No, Date): US 73209 980130
DESIGNATED STATES: AT; BE; CH; CY; DE; DK; ES; FI; FR; GB; GR; IE; IT; LI; LU; MC; NL; PT; SE
INTERNATIONAL PATENT CLASS: **G06F-017/30** ; **G06F-003/14**
NOTE:
No A-document published by EPO
LEGAL STATUS (Type, Pub Date, Kind, Text):

Application:	001108 A1	Published application with search report
Application:	991006 A1	International application. (Art. 158(1))
Withdrawal:	040204 A1	Date application deemed withdrawn: 20030801
Examination:	001108 A1	Date of request for examination: 20000713
Search Report:	010425 A1	Date of drawing up and dispatch of supplementary:search report 20010308
Application:	991006 A1	International application entering European phase

LANGUAGE (Publication,Procedural,Application): English; English; English

2/5/2 (Item 1 from file: 349)
DIALOG(R)File 349:PCT FULLTEXT

00507933 **Image available**
SYSTEM AND METHOD FOR CREATING AND MANIPULATING INFORMATION CONTAINERS WITH DYNAMIC REGISTERS
SYSTEME ET PROCEDE POUR LA CREATION ET LA MANIPULATION DE CONTENEURS D'INFORMATIONS A REGISTRES DYNAMIQUES
Patent Applicant/Assignee:
EMATRIX CORPORATION,
DE ANGELO Michael,
Inventor(s):
DE ANGELO Michael
Patent and Priority Information (Country, Number, Date):
Patent: WO 9939285 A1 19990805
Application: WO 99US1988 19990128 (PCT/WO US9901988)
Priority Application: US 9873209 19980130
Designated States:

(Protection type is "patent" unless otherwise stated - for applications prior to 2004)
AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW GH GM KE LS MW SD SZ UG ZW AM AZ BY KG KZ MD RU TJ TM AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE BF BJ CF CG CI CM GA GN GW ML MR NE SN TD TG

Main International Patent Class: **G06F-017/30**
International Patent Class: **G06F-003/14**
Publication Language: English
Fulltext Availability:
Detailed Description
Claims
Fulltext Word Count: 18390

English Abstract
A system for creating and manipulating information containers with dynamic registers on a multi-user computer system, or computer network comprises an interactive information container, a container editor, a search interface, a user profile, system-wide hierarchical container gateways (site 7), interactive and evolving container registers, a data collection means, a data reporting means, an analysis engine with editor, an executing engine with editor, and a means of communicating with other computers, computer networks, or digital-based public or published media. The container editor provides an authoring user with the capacity to encapsulate any information component such as a file, set, database, network, event or process, and a set of parameters of multiple container registers to govern the interaction of that container with other containers or processes. The container registers include system-defined, system-alterable, user-defined and user-alterable registers.

French Abstract
L'invention concerne un systeme pour la creation et la manipulation de conteneurs d'informations a registres dynamiques, sur un systeme informatique multi-utilisateur, ou sur un reseau informatique. Ce systeme comprend un conteneur d'informations interactif, un editeur de conteneur, une interface de recherche, un profil d'utilisateur, des passerelles (site 7) de conteneurs hierarchiques a l'echelle du systeme, des registres interactifs et evolutifs, un dispositif de rassemblement de donnees, un dispositif d'edition de donnees, un moteur d'analyse avec editeur, un moteur d'execution avec editeur, et un dispositif permettant de communiquer avec d'autres ordinateurs, avec des reseaux informatiques, ou avec des supports numeriques publics ou publies. L'editeur de conteneur permet a un utilisateur-auteur d'encapsuler n'importe quel composant d'information tel qu'un dossier, un ensemble, une base de donnees, un reseau, un evenement ou un procede, et fournit a cet utilisateur une serie de parametres pour plusieurs registres de conteneurs pour commander l'interaction de ce conteneur avec d'autres conteneurs ou procedes. Les registres de conteneurs comprennent des registres definis par le systeme, modifiables par le systeme, definis par l'utilisateur et modifiables par l'utilisateur.

2/5/3 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

012673114 **Image available**
WPI Acc No: 1999-479221/199940
XRPX Acc No: N99-356757

Computer system for creating and manipulating information containers in multi-user systems e.g. client server network

Patent Assignee: EMATRIX CORP (EMAT-N)
Inventor: **DE ANGELO M**
Number of Countries: 085 Number of Patents: 003
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Week	
WO 9939285	A1	19990805	WO 99US1988	A	19990128	199940	B
AU 9925687	A	19990816	AU 9925687	A	19990128	200002	
EP 1049996	A1	20001108	EP 99905548	A	19990128	200062	
			WO 99US1988	A	19990128		

Priority Applications (No Type Date): US 9873209 P 19980130
Patent Details:

Patent No	Kind	Lan	Pg	Main IPC	Filing Notes
WO 9939285	A1	E	78	G06F-017/30	

Designated States (National): AL AM AT AU AZ BA BB BG BR BY CA CH CN CU CZ DE DK EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT UA UG US UZ VN YU ZW
Designated States (Regional): AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SZ UG ZW

AU 9925687	A		G06F-017/30	Based on patent WO 9939285
EP 1049996	A1	E	G06F-017/30	Based on patent WO 9939285

Designated States (Regional): AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

Abstract (Basic): WO 9939285 A1

NOVELTY - A container editor provides an authoring user with the capacity to encapsulate any information component such as a file, set, database, network, event or process, and a set of parameters of multiple container registers to govern the interaction of that container with other containers or processes. The container-registers include system-defined, system-alterable, user-definable and user-alterable algorithms.

DETAILED DESCRIPTION - INDEPENDENT CLAIMS are included for; a method for creating an interactive information container; a method for interacting between two interactive information containers.

USE - Transmitting, receiving and manipulating information containers with dynamic registers on a multi-user computer system, or computer network e.g. local, wide area or public networks, in computer, media or publishing networks.

ADVANTAGE - Information can be manufactured on, utility upgraded, and intelligence developed in a computer network by offering the mechanism to create and manipulate information containers with dynamic registers.

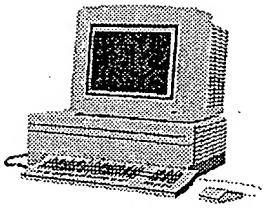
DESCRIPTION OF DRAWING(S) - The drawing shows a block diagram of a preferred embodiment of the invention.

pp; 78 DwgNo 1/17

Title Terms: COMPUTER; SYSTEM; MANIPULATE; INFORMATION; CONTAINER; MULTI; USER; SYSTEM; CLIENT; SERVE; NETWORK
Derwent Class: T01
International Patent Class (Main): **G06F-017/30**
International Patent Class (Additional): **G06F-003/14**
File Segment: EPI

EIC2100

Search Results Feedback Form (Optional)



Scientific & Technical Information Center

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Anne Hendrickson, Team Leader, 571-272-3490, RND 4B28
or Carol Wong, Librarian, 571-272-3513, RND 4B28

Voluntary Results Feedback Form

- *I am an examiner in Workgroup:* ☐ *Example: 2170*
- *Relevant prior art **found**, search results used as follows:*
  - ☐ 102 rejection
  - ☐ 103 rejection
  - ☐ Cited as being of interest.
  - ☐ Helped examiner better understand the invention.
  - ☐ Helped examiner better understand the state of the art in their technology.

Types of relevant prior art found:

- ☐ Foreign Patent(s)
- ☐ Non-Patent Literature
  (journal articles, conference proceedings, new product announcements etc.)

- *Relevant prior art **not found**:*
  - ☐ Results verified the lack of relevant prior art (helped determine patentability).
  - ☐ Search results were not useful in determining patentability or understanding the invention.

Other Comments:

Drop off or send completed forms to **STIC/EIC2100 RND 4B28.**